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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/737,783	12/15/2000	Perry Wang	42390P9634	2478

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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,783	WANG ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 11/28/2005.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The abstract of the disclosure is objected to because it is grammatically incorrect. For instance, the phrase "by one of a multiple predicated instructions" is worded incorrectly. In addition, the phrase "an instruction renaming is deferred" is worded incorrectly, and the phrase "by injecting of one or more micro-operations" is worded incorrectly. Correction is required. See MPEP § 608.01(b).

5. The disclosure is objected to because of the following informalities: On page 10, line 1, it is not clear what is meant by "postpones the predicated instructions down the pipeline...". What is postponed? Should this word be replaced with "propagated"?

Appropriate correction is required.

Drawings

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

In Fig.2, the examiner has been unable to find reference numbers 205, 215, 220, 225, and 230 in the specification.

In Fig.2A, the examiner has been unable to find reference numbers 254 and 262 in the specification.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-8 and 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. More specifically, applicant is claiming that register renaming is deferred in claims 1 and 14, but it is not clear how the renaming can be considered deferred. The examiner understands that a consumer instruction does not have to be stalled in the rename stage while predicates are being resolved, but to defer means to postpone or put off for some time, and it is not clear when the renaming is postponed to. For example, looking at the example in Fig.6, the examiner assumes that in the rename stage, the destination of the select-uop is changed to rD, and the destination of the consumer (mov) instruction is changed to rZ and its source to rD so that the source will be obtained from the result of the select-uop. However, the examiner is not clear as to when any additional renaming for these instructions occurs. That is, the deferral of renaming for these instructions is not evident from the specification/drawings. Applicant is asked to clarify the claims.

9. Claim 2 recites the limitation "the pipeline instruction" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-6 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dabbagh et al., U.S. Patent No. 6,701,425 (herein referred to as Dabbagh).

12. Referring to claim 1, Dabbagh has taught a microprocessor comprising:

a) a unit to insert a first micro-operation into an instruction stream. See column 6, line 42, to column 7, line 8. Note that a send guard instruction is inserted into the stream to transfer the predicate/guard value to the unit that needs to analyze the predicate. In an alternate interpretation, any other instruction inserted between a producer and consumer will qualify as the first micro-operation.

b) while injecting the first micro-operation does inherently defer processing of subsequent instructions, Dabbagh has not taught deferring renaming of a plurality of register defined by predicate instruction upon which a common instruction depends. However, Official Notice is taken that register renaming is a well-known concept which allows for a reduction in hazards, and consequently, processor stalling. Clearly, if an extra instruction is injected into the stream, then the processing is stalled at least one clock cycle for all subsequent instructions. And, since renaming is part of the processing pipeline, the renaming would be deferred at least a cycle as well. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dabbagh to include a register renamer for renaming registers accessed by instructions. Furthermore, it should be realized that any subsequent instruction can access registers defined by a predicated instruction. For instance, the program may have two consecutive predicated arithmetic operations, one which writes to register R1 and another which writes a result to register R2. Then a consumer instruction could follow, if the programmer so desires which reads both R1 and R2, performs an arithmetic operation on them, and then stores the result in register R3. Therefore, merely claiming an instruction sequence is not a patentable feature. An infinite number of program sequences may exist and it is known to have consumers

follow producers. And, in a system with register renaming, consumers must have their registers renamed as well.

c) as discussed above Dabbagh has not taught a plurality of register renaming units (or an augmented register alias table) to rename at least one register corresponding to the predicated instructions wherein the common instruction is to use data from a plurality of destination registers corresponding to the first micro-operation. However, for the reasons discussed above, this is also an obvious modification to Dabbagh. It would be obvious to have register renaming units (and augmented alias table) to track and rename registers corresponding to predicated instructions. A consumer will also be using data from a destination register that is associated with the predicate that is transferred by the first micro-operation (in the case of a send guard instruction) or may be a consumer of the first micro-operation (reads the producer's destination).

13. Referring to claim 2, Dabbagh has taught a microprocessor as described in claim 1. Furthermore, if Dabbagh includes register renaming as set forth above, then Dabbagh also has taught that a register renaming unit renames each one of a plurality of source registers of the pipeline instruction and renames a destination register to a new physical register. This is another concept that occurs with register renaming. Each original destination is renamed to a new destination, and subsequent instructions that access the original destination as a source, must have that source renamed to the new destination as well.

14. Referring to claim 3, Dabbagh has taught a microprocessor as described in claim 2. Furthermore, if Dabbagh includes register renaming as set forth above, then Dabbagh also has taught that the augmented register alias table includes a plurality of lines and wherein each one

of the plurality of lines includes a plurality of renamed destination registers. Again, if a renaming system is employed, then there must be a table which tracks and maps the registers.

15. Referring to claim 4, Dabbagh has taught a microprocessor as described in claim 3. Dabbagh has further taught that each one of a plurality of select-uops has a plurality of source operands wherein each one of the plurality of source operands corresponds to a physical register identifier. Clearly, Dabbagh executes arithmetic-type operations such as Adds and Subs (Fig.1). These operations are known to access multiple source registers.

16. Referring to claim 5, Dabbagh has taught a microprocessor as described in claim 4. Dabbagh has further taught that the plurality of source operands comprises a first source operand and a plurality of secondary source operands. Again, it is known that when an ADD instruction is executed, two operands may be two register operands (add two numbers to get a result).

17. Referring to claim 6, Dabbagh has taught a microprocessor as described in claim 5. Dabbagh has further taught that the first source operand includes a default physical register identifier, wherein the default physical register is always valid and available. The ADD instruction source must be valid and available otherwise the program would execute with incorrect data (and produce incorrect results).

18. Referring to claim 14, Dabbagh has taught a computer system comprising a processor, wherein the processor includes:

a) a unit to insert a first micro-operation into an instruction stream. See column 6, line 42, to column 7, line 8. Note that a send guard instruction is inserted into the stream to transfer the predicate/guard value to the unit that needs to analyze the predicate. In an alternate

interpretation, any other instruction inserted between a producer and consumer will qualify as the first micro-operation.

b) the first micro-operation to defer renaming of a plurality of registers defined by different predicated instructions, upon which a dependent instruction depends. However, Official Notice is taken that register renaming is a well-known concept which allows for a reduction in hazards, and consequently, processor stalling. Clearly, if an extra instruction is injected into the stream, then the processing is stalled at least one clock cycle for all subsequent instructions. And, since renaming is part of the processing pipeline, the renaming would be deferred at least a cycle as well. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dabbagh to include a register renamer for renaming registers accessed by instructions. Furthermore, it should be realized that any subsequent instruction can access registers defined by a predicated instruction. For instance, the program may have two consecutive predicated arithmetic operations, one which writes to register R1 and another which writes a result to register R2. Then a consumer instruction could follow, if the programmer so desires which reads both R1 and R2, performs an arithmetic operation on them, and then stores the result in register R3. Therefore, merely claiming an instruction sequence is not a patentable feature. An infinite number of program sequences may exist and it is known to have consumers follow producers. And, in a system with register renaming, consumers must have their registers renamed as well.

c) a plurality of execution units to execute the dependent instruction. See Fig. 1.

d) While Dabbagh has not explicitly taught a reorder buffer, Official Notice is taken that reorder buffers are well known in the art. They allow for the reordering of instructions that have been

executed out of order, which further allows for increased throughput. As a result, it would have been obvious to implement a reorder buffer in Dabbagh to achieve out of order execution.

e) as mentioned above, Dabbagh has not taught a plurality of register renaming units (or augmented register alias table) to rename at least one register corresponding to a predicated instruction, wherein the dependent instruction is to use data from a plurality of destination registers corresponding to the first micro-operation. However, for the reasons discussed above, this is also an obvious modification to Dabbagh. It would be obvious to have register renaming units (and augmented alias table) to track and rename registers corresponding to predicated instructions. A consumer will also be using data from a destination register that is associated with the predicate that is transferred by the first micro-operation (in the case of a send guard instruction) or may be a consumer of the first micro-operation (reads the producer's destination).

f) Dabbagh has not taught a plurality of reservation stations, however Official Notice is taken that reservation stations are well known in the art. They provide efficient operand tracking and scheduling of instructions. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dabbagh to include a plurality of reservation stations.

g) wherein a register renaming unit, the reorder buffer, the plurality of execution units, and the plurality of reservation stations are coupled to at least one of a plurality of dynamic pipeline stages. it is inherent that all logic in a processor is coupled to a pipeline, which is inherently made of stages.

h) a system bus. See Fig.1

i) a computer memory system. See Fig.1, Fig.3, and Fig.4.

j) an input/output device. See the register files of Fig.1. Registers receive input and supply output and are therefore I/O devices.

k) wherein the system bus is coupled to the processor, the computer memory system and the input/output device. See Fig.1.

19. Referring to claim 15, Dabbagh has taught a computer system as described in claim 14. Furthermore, claim 15 is rejected for the same reasons set forth in the rejection of claim 3.

20. Referring to claim 16, Dabbagh has taught a computer system as described in claim 15. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 2.

21. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dabbagh, as applied above, in view of Fetterman et al., U.S. Patent No. 5,553,256 (herein referred to as Fetterman).

22. Referring to claim 7, Dabbagh has taught a microprocessor as described in claim 5. While Dabbagh has inherently taught that each operand includes a physical status identifier (the registers must be identified via address specifier), Dabbagh has not taught that each one of the plurality of second source operands includes a plurality of status bits. However, Fetterman has taught associating status bits with register operands to track their progress. See Fig.2, bits S1V and S2V, column 9, lines 40-42, and column 4, lines 52-58, and note that one bit tracks readiness and the other tracks when it's been written to (commit bit).

23. Referring to claim 8, Dabbagh in view of Fetterman has taught a microprocessor as described in claim 7. Dabbagh in view of Fetterman has further taught that the plurality of status bits has a ready bit and a committed bit. See the rejection of claim 7.

Allowable Subject Matter

24. Claims 9-13 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
February 9, 2006

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